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CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

EXAMINER
CHO, JAMES HYONCHOL

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/605,312	WRIGHT, ANDREW J.	
	Examiner	Art Unit	
	James H. Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Receipt is acknowledged of the Amendment filed May 5, 2003.

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on May 5, 2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Objections

3. Claim 20 is objected to because of the following informalities: "said control signal" on line 10 and 14 appears to be --said input signal-- respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-8, 10-13 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Sharpe-Geisler (US PAT No. 6,359,466).

Regarding claim 1, Figs. 5 and 8 of Sharpe-Geisler discloses an apparatus comprising a polarity switch (510 in Fig. 5; details of switch in shown in Fig. 8)

comprising a first memory cell (LUT 502 has memory cells as shown in Fig. 1; col. 3, lines 66-67) connected to an input terminal (output of memory cell is connected to the input terminal 1 via a multiplexer) of a first transmission gate (pass gate comprising 700 and 800) and a second memory cell (LUT 504) connected to an input terminal (input terminal 0) of a second transmission gate (pass gate comprising 702 and 802) where an input signal (signal on SEL) of the polarity switch is presented to a first control terminal (SEL) of the first and second transmission gates and an output (output of 510) of the polarity switch is configurable in response to signals at the input terminals of the first and second transmission gate to present either

a signal that varies in response to the input signal (if signals at terminals 1 and 0 is (0,1), the output changes to a logic 1 if SEL is a logic low or a logic 0 if SEL is a logic high, and if signals at terminals at 1 and 0 is (1,0), the output changes to a logic 0 if SEL is a logic low or a logic 1 if SEL is a logic high) or

a predetermined logic level that is independent of the input signal (if signals at terminals 1 and 0 is (0,0), the output stays a logic 0 independent of SEL, and if signals at terminals 1 and 0 is (1,1), the output stays a logic 1 independent of SEL).

Regarding claim 2, Figs. 5 and 8 of Sharpe-Geisler discloses the apparatus according to claim 1 where the first and second transmission gates further comprise a second control terminal (output of inverter 704 in Fig. 8) configured to receive a complement of the input signal (inverter 704 is complement of SEL).

Regarding claim 3, Figs. 5 and 8 of Sharpe-Geisler discloses the apparatus according to claim 1 where the first and second memory cells comprise a first configuration and a second configuration bit of the apparatus (LUT 502 and 504 stores and provides configuration bits based on inputs as shown in Fig. 2).

Regarding claim 4, Figs. 5 and 8 of Sharpe-Geisler discloses the apparatus according to claim 1 where an output terminal of the first transmission gate and an output terminal of the second transmission gate are connected to the output of the polarity switch (output of 700, 800 and 702, 802 are connected to the output of 506 in Fig. 8).

Regarding claim 5, Figs. 5 and 8 of Sharpe-Geisler discloses the apparatus according to claim 1 where the input signal comprises an input term (signal SEL is an input term for 506 in Fig. 8), and the output is configured to present a product term input (the output of 506 is a product term input for the next stage as shown in Fig. 5).

Regarding claim 6, Figs. 5 and 8 of Sharpe-Geisler teaches an apparatus comprising a first circuit (700 and 800 in Fig. 8) configured to present a first value stored in a first memory cell (LUT 502 has memory cells as shown in Fig. 1; col. 3, lines 66-67) to an input node (the output of 510 is an input to an another stage) in response to a first state of an input signal (SEL); and a second circuit (702 and 802 in Fig. 8) configured to present a second value stored in a second memory cell (LUT 504 in Fig. 5) to the input

node in response to a second state of the input signal (SEL) where the first and second stored values are programmable during configuration of the apparatus (memory cell are programmed in any arbitrary manner; col. 1, lines 27-29).

Regarding claim 7, Figs. 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 6, where the first and second circuits each comprise the first and second memory cells coupled to an input terminal of a first and a second transmission gates (700 and 800 comprises a transmission gate, and 702 and 802 comprises another transmission gate).

Regarding claim 8, Figs. 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 7 where the transmission gates comprise a CMOS transistor pair (PMOS 800 and NMOS 700, PMOS 802 and NMOS 702 in Fig. 8).

Regarding claim 10, Figs. 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 7, where the output of the apparatus presents a predetermined logic level when the memory cells of the first and second circuits contains the same data (if signals at terminals 1 and 0 is (0,0), the output stays a logic 0 independent of SEL, and if signals at terminals 1 and 0 is (1,1), the output stays a logic 1 independent of SEL) and a signal that varies in response to the input signal when the memory cells contain different data (if signals at terminals 1 and 0 is (0,1), the output changes to a logic 1 if SEL is a logic low or a logic 0 if SEL is a logic high, and if signals at terminals at 1 and 0

is (1,0), the output changes to a logic 0 if SEL is a logic low or a logic 1 if SEL is a logic high).

Regarding claim 11, Figs. 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 10 where data comprises configuration data (LUT 502 and 504 stores and provides configuration bits based on inputs as shown in Fig. 2).

Regarding claim 12, Figs. 5 and 8 of Sharpe-Geisler teaches discloses the apparatus according to claim 7, where the memory cells are configured to source or sink a current (it is inherent that when the output of 502 and 504 is high, 502 and 504 source a current while they sink a current when the output of 502 and 504 is low).

Regarding claim 13, Figs. 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 6, where the apparatus comprises a product term input circuit of a programmable logic device (LUT 502, 504 are programmable logic device and provides a product term input circuit; col. 1, lines 20-35).

Regarding claim 15, Figs. 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 6 where the input signal comprises an input term (signal SEL is an input term for 506 in Fig. 8).

Regarding claim 16, Figs. 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 15 where the apparatus is programmable to present any of the input term (when signals at terminals at 1 and 0 is (1,0), the output follows the SEL signal, i.e. the output is a logic 0 if SEL is a logic low or a logic 1 if SEL is a logic high), a digital complement of the input term (when signals at terminals 1 and 0 is (0,1), the output is complement of SEL, i.e. the output is a logic 1 if SEL is a logic low or a logic 0 if SEL is a logic high) and a predetermined logic level to the input node (if signals at terminals 1 and 0 is (0,0), the output stays a logic 0 independent of SEL, and if signals at terminals 1 and 0 is (1,1), the output stays a logic 1 independent of SEL).

Regarding claim 17, Figs. 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 16 where the predetermined logic level is selectable from a digital 0 or a digital 1 (if signals at terminals 1 and 0 is (0,0), the output stays a logic 0 independent of SEL, and if signals at terminals 1 and 0 is (1,1), the output stays a logic 1 independent of SEL).

Regarding claim 18, Figs. 5 and 8 of Sharpe-Geisler teaches a method for providing a product term input of a programmable logic device (Fig. 5 is a programmable logic device having LUT and memory cells) comprising the steps of:

presenting a first value stored in a first memory cell to an input node (output of 506) in response to a first state of an input signal (SEL; LUT 502 has memory cells as shown in Fig. 1 and one memory cell content is outputted to an input terminal 1 of 506

in Fig. 8 via a multiplexer, and 506 presents the content of the memory cell to the output of 506 in response to the SEL signal ; col. 3, line 66 - col. 4, line 17), and presenting a second value stored in a second memory cell to the input node in response to a second state of the input signal, (LUT 504 has memory cells as shown in Fig. 1 and one memory cell content is outputted to an input terminal 0 of 506 in Fig. 8 via a multiplexer, and 506 presents the content of the memory cell to the output of 506 in response to the SEL signal ; col. 3, line 66 - col. 4, line 17), where the first and the second stored values are programmed during configuration of the programmable logic device (memory cell are programmed in any arbitrary manner; col. 1, lines 27-29).

Regarding claim 19, Figs. 5 and 8 of Sharpe-Geisler teaches the method according to claim 18, where the input signal comprises an input term of a logic block of the programmable logic device (SEL is an input term of a logic block comprising 514 and configuration memory 518).

Regarding claim 20, Figs. 5 and 8 of Sharpe-Geisler teaches the method according to claim 18, further comprising the steps of:

generating a first logic level (logic 1) at the input node in response to the first and the second stored values being programmed with a first value (logic 1; if signals at terminals 1 and 0 is (1,1), the output stays a logic 1); generating a second logic level (logic 0) at the input node in response to the first and the second stored values being programmed with a second value (logic 0; if signals at terminals 1 and 0 is (0,0), the

output stays a logic 0); generating a signal at the input node that has a state similar to the input signal in response to the first stored value being programmed with the first value and the second stored value being programmed with the second value (if signals at terminals at 1 and 0 is (1,0), the output follows the SEL signal); and generating a signal at the input node that has a state similar to a digital complement of the input signal in response to the first stored value being programmed with the second value and the second stored value being programmed with the first value (if signals at terminals 1 and 0 is (0,1), the output is complement of SEL).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sharpe-Geisler in view of Bauer (US PAT No. 5,889,413).

Regarding claim 9, Figs. 5 and 8 of Sharpe-Geisler discloses teaches the apparatus according to claim 7, but does not disclose the first and the second circuits comprise a first and a second CMOS inverters coupling the first and second memory cells to the first and the second transmission gates.

However, Fig. 1 of Bauer discloses a CMOS inverter (726) coupled to the output of a memory cell (700) for the purpose of increasing the drive of the memory cell (col. 1, lines 45-47).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to add a CMOS inverter of Bauer at the memory cell output of Sharpe-Geisler because it would provide increased driving strength.

6. Claim 14 is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Sharpe-Geisler in view of Silver (US PAT No. 5,952,846).

Regarding claim 14, Figs 5 and 8 of Sharpe-Geisler teaches the apparatus according to claim 6, but does not disclose an AND plane of a programmable logic device comprising one or more apparatus according to claim 6. However, this limitation appears to be merely a statement of intent of the apparatus to be used in the AND plane of the programmable logic device. It has been held that a recitation directed to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

However, if the limitation regarding the intended use of the apparatus in the AND plane of the programmable logic device is not considered a mere statement of intended use as discussed above, Figs. 1 and 2 of Silver discloses a complex programmable logic devices (CPLD) including an AND array, i.e. AND plane, two or more function

blocks for the purpose of providing a circuit designer the convenience of implementing a complex logic function using a single IC and reduction in the cost and size of the IC. (col. 1, lines 48-62).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to implement the one or more apparatus of Sharpe-Geisler in a CPLD including an AND array, i.e. AND plane of Silver because it would provide design flexibility that is inherent in a programmable logic device and reduction in the cost and size of the IC.

Response to Arguments

7. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James H. Cho whose telephone number is 703-306-5442. The examiner can normally be reached on Monday-Friday, 05:30am-02:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

James H. Cho
Examiner
Art Unit 2819

July 25, 2003